IN THE CLAIMS

1. (Original) A system comprising:

a buffer;

a wavelet transform unit having an input coupled to the buffer to perform a reversible wavelet transform on pixels stored in the buffer and to generate coefficients at an output;

a coder coupled to the wavelet transform unit to code bitplanes of wavelet transformed pixels from the wavelet transform unit and stored bitplanes of wavelet transformed pixels received from the buffer, wherein the coder comprises

a context model, and

a parallel entropy coder encoder, and

wherein the most important data is not embedded and is coded in coefficient order without buffering, a portion of less important data is buffered, embedded and written to memory in order of importance.

2. (Original) The system defined in Claim 1 wherein the buffer comprises a band buffer to store at least one band of pixels

3. (Original) The system defined in Claim 1 wherein the encoder comprises a high speed parallel coder.

4. (Original) The system defined in Claim 1 wherein the encoder comprises a QM-coder.

5. (Original) The system defined in Claim 1 where the encoder comprises a finite state

machine coder.

6. (Original) The system defined in Claim 1 further comprising a coded data interface.

7. – 33. (Canceled)

34. (Currently Amended) An integrated circuit (IC) chip comprising:

a pixel data interface to transfer pixel data between the IC chip and memory;

a reversible wavelet transform coupled to the pixel data interface to transfer information to and from the memory via the pixel data interface;

a context model coupled to the reversible wavelet transform to provide contexts for coding the data provided therefrom; and

an encoder to encode coefficients generated by the reversible wavelet transform based on contexts provided by the context model, wherein the encoder encodes a first data of coefficients in a set of coefficients in coefficient order, and wherein the encoder then encodes a second data and embeds the second data by order based, in part, on a plurality of signaling bits, the first data having a higher priority than the second data.

35. (Original) The IC defined in Claim 34 further comprising a coefficient data interface coupled to transfer coefficients from the transform to the memory without coding.

36. (Original) The IC defined in Claim 34 wherein the coefficient data interface transfers coefficients from memory to the context model for encoding.

37. (Original) The IC defined in Claim 34 further comprising a coded data interface for providing entropy coded data to memory.

38. (Original) The IC defined in Claim 37 further comprising a decoder to decode encoded data.

39. (Original) The IC defined in Claim 36 further comprising a coded data interface to provide the decoder with entropy coded data for decoding.

40. (Original) The IC defined in Claim 34 further comprising a reversible color space converter coupled between the pixel data interface and the reversible wavelet transform to perform reversible color space conversion.

41. – 47. (Canceled)

48. (Currently Amended) A system comprising:

a context model;

a probability estimation machine coupled to the context model;

a bit generator coupled to the probability estimation machine; and

an encoder rate control coupled to an output of the bit generator to control the encoding rate by determining average codeword length, wherein the encoder rate control encodes a first data of coefficients in a coefficient order, and wherein the encoder rate control then encodes a second data and embeds the second data by order based, in part, on a plurality of signaling bits, the first data having a higher priority than the second data.

49. (Original) The system defined in Claim 48 wherein an encoder rate control adjusts quantization.

50. (Original) The system defined in Claim 48 comprising a signaling block to signal a decoder regarding a new quantization level.

51. (Original) The system defined in Claim 48 further comprising a signaling block to generate header data for a compressed data stream output of the encoder which is concatenated onto the compressed bit stream to indicate to the decoder a new level of quantization.

52. (Original) The system defined in Claim 48 wherein the encoder rate control stores an indication of the quantization level is necessary for subsequent use by the decoder.

53. – 79 (Canceled)

80. (Currently Amended) A system comprising:

modeling means for providing contexts;

probability estimating means for providing probability estimates in response to contexts from the context model;

bit generation means for providing zero or more bits in response to probability estimates from the probability estimating means; and

encoder rate control means for coupled to an output of the bit generation means for controlling the encoding rate by determining average codeword length, wherein the encoder rate control means encodes a first data of coefficients in a coefficient order, and wherein the encoder rate control means then encodes a second data and embeds the second data by order based on at least one or more signaling bits, the first data having a higher importance than the second data.

81. (Original) The system defined in Claim 80 wherein an encoder rate control means adjusts quantization.

82. (Original) The system defined in Claim 80 further comprising means for signaling a decoder regarding a new quantization level.

83. (Original) The system defined in Claim 80 further comprising means for generating header data for a compressed data stream output of the encoder which is concatenated onto the compressed bit stream to indicate to the decoder a new level of quantization.

84. (Original) The system defined in Claim 80 wherein the encoder rate control means stores an indication of the quantization level is necessary for subsequent use by the decoder.

85. (Original) The method defined in Claim 34 wherein the encoder codes bit planes of wavelet transformed pixels from the reversible wavelet transform and stored bit planes of wavelet transform pixels.

86. (Currently Amended) ~~The method defined in Claim 34~~ An integrated circuit (IC) chip comprising:

a pixel data interface to transfer pixel data between the IC chip and memory;

a reversible wavelet transform coupled to the pixel data interface to transfer information to and from the memory via the pixel data interface;

a context model coupled to the reversible wavelet transform to provide contexts for coding the data provided therefrom; and

an encoder to encode coefficients generated by the reversible wavelet transform based on contexts provided by the context model,

wherein the encoder codes the most important data of coefficients in a set of coefficients immediately in coefficient order and then codes the less important data and embeds the less important data by order based, in part, on a plurality of signaling bits.

87. – 91. (Canceled)